REMARKS

Reconsideration of the application is requested.

Applicants acknowledge the Examiner's confirmation of receipt of applicants' certified copy of the priority document for the German Patent Application 198 43 640.8, filed September 23, 1998 supporting the claim for priority under 35 U.S.C. § 119.

Claims 1-26 are in the application. Claims 1-17 and 19-26 were rejected and claim 18 was objected to in the above-identified Office Action.

In "Drawings" item 2 on page 2 of the above-identified Office Action, Fig. 11 was objected to because one item was labeled "Precode Unit" instead of "Predecode Unit". The Examiner's suggested corrections have been made.

In "Claim Rejections - 35 USC § 103" item 4 on page 2 of the above-identified Office Action, claims 1 and 6-13 have been rejected as being obvious over Applicants Alleged Admitted Prior Art (hereinafter **AAAPA**) in view of U.S. Patent No. 5,946,219 to *Mason, et al.* (hereinafter **MASON**) under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103" item 11 on page 4 of the above-identified Office Action, claims 2-5, 14-17, and 19-26 have been rejected as being obvious over **AAAPA** in view of **MASON** and further in view of U.S. Patent No. 6,077,315 to *Greenbaum, et al.* (hereinafter **GREENBAUM**) under 35 U.S.C. § 103.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a method for configuring a configurable hardware block including:

(a) implementing one of commands and command sequences of a program to be executed, the implementing step includes:

(a1) **ascertaining a given type of subunit of a configurable hardware block**, the given type of subunit being required for executing a respective command;

(a2) **selecting, if available, a subunit** of the given type of subunit;

(a3) **configuring** configurable **connections** provided **around the subunit** selected in the selecting step, if the subunit of the given type of subunit is found in the selecting step;

(b) ascertaining configuration data with the step of implementing the one of commands and command sequences; and

(c) configuring the configurable hardware block by using the configuration data.

Independent Claim 24 calls for, *inter alia*, a method for configuring a configurable hardware block including:

> attempting to **form pseudo-hyperblocks** including a plurality of hyperblocks **when implementing commands as configuration data**; and
>
> **configuring a configurable hardware block** by using the configuration data

The **AAAPA** reference found in the specification of the instant application discloses a block diagram of the basic structure of an >S<puter. Specifically, contrary to the Examiner's assertion in item 5a on page 2 of the above-identified Office Action, the **AAAPA** only provides a partial block diagram of the >S<puter and expressly indicates that only the part that process the commands is shown. More specifically, the specification clarifies that the only configurable hardware block included in the s-unit 4 of the >S<puter is the functional unit 42. For example, page 2, lines 4-24 of the specification of the instant application states:

> It should be noted that **the >S<puter, in particular its part which processes the commands, is shown and described only in part (only to the extent significant for the configurable hardware blocks considered in more detail in the present case, and for their configuration)**.

> **The >S<puter shown in Fig. 11** includes a predecode unit 1, an instruction buffer 2, a decode, rename & load unit 3, **the aforementioned s-unit 4**, a data cache 5 and a memory interface 6, *the s-unit 4 including a programmable structure buffer 41,* ***a functional unit with programmable structure 42,*** *an integer/address instruction buffer 43 and an integer register file 44.*
>
> The particular feature of the >S<puter is, in particular, its s-unit 4, more precisely the functional unit 42 thereof. **The functional unit 42 is a piece of configurable hardware** which, on the basis of commands or command sequences which are to be executed by the >S<puter, **can be dynamically configured such that it is able to execute the actions and operations prescribed by the commands or command sequences.**

The express language of the specification explicitly contradicts the Examiner's assumptions in item 5, namely that **AAAPA** teaches "configuring a configurable hardware block … **ascertaining a given type of subunit** of a configurable hardware block … configuring configurable connections provided **around the subunit** … and configuring the configurable hardware block by using the configuration data." as recited in claim 1 of the instant application. In fact, the **AAAPA only indicates** that functional unit 42 **"can be dynamically configured** such that it is able to execute the actions and operations prescribed by the commands or command sequences." The claimed configuration steps of the instant application may clearly only be performed inside of functional unit 42 and NOT the s-unit 4 as indicated by the Examiner.

Moreover, it is important to note that the background language does not indicate that the s-unit 4 or the functional unit 42 **have** (past tense) been configured according to the claims of the instant application, rather prophetic language is used, namely "The functional unit 42 is a piece of configurable hardware which … **can be dynamically configured** such that it is able to execute the actions and operations prescribed by the commands or command sequences" page 2, lines 19-24. Without further outside support for the Examiner's position, the applicants respectfully submit that the Examiner should include the "can be" functionality of the >S<puter as part of the present invention and not part of the **AAAPA**.

Applicants also respectfully reiterate that the >S<puter "**is shown and described only…to the extent significant for the configurable hardware blocks considered in more detail in the present case, and for their configuration**" and therefore although parts of the structure existed previously, the specific combination as outlined in the instant application is still believed to be unique.

In fact, as previously indicated, the specification expressly states that "The functional unit 42 is a piece of configurable hardware" not a given type of subunit as

asserted by the Examiner. This is significant as the "given type of subunit" are actually configurations of the "function unit 42" as detailed in specification of the instant application. Furthermore, the missing limitations of the **AAAPA** as outlined by the Examiner on page 3 in items 5, e-g of the above-identified Office Action must also be interpreted as "a given type of subunit of a configurable hardware block" where the functional unit 42 and not the s-unit 4 is the configurable hardware block in relation to **MASON**.

The **MASON** reference discloses configuring an array of logic devices. More specifically, **MASON** discloses a dynamically reconfigurable FPGA where only selected portions of the logic array may be reconfigured. This allows changes to be made to an FPGA without having to program the entire device.

MASON does not teach or suggest, "ascertaining a given type of subunit of a configurable hardware block" as recited in claim 1 of the instant application. Rather **MASON** only discloses the general use of dynamically reconfigurable FPGAs to create available configurations (Col. 1, line 45 - Col. 2, lines 41) but the term "ascertaining" as recited in claim 1 of the instant application implies that "the given type of subunit" is discovered or determined through some

experimentation or examination based the requirements "for executing a respective command" relative to available subunits in the configurable hardware block. Once a particular type is ascertained, a further determination is made whether the particular subunit is "available" for configuration. As indicated in the specification, a subunit may be unavailable for a variety of reasons. For example, the desired subunit may be in use by another virtual unit. Thus a desired subunit may be either "not available or no longer available" (page 8, lines 4 and 5) and is only selected for further configuration "if available" as recited in claim 1 of the instant application.

Moreover, **MASON** includes no indication or discussion of how configurations are ascertained and later provisionally executed based on their respective availability. Nor does **MASON** provide information about how the connections around the subunit are selected, rather the applicants respectfully assert that **MASON** explicitly teaches away from this limitation by indicating that "only selected portions of the array" are permitted to be reconfigured (Col. 2, lines 1-2). In contrast, once the given type is ascertained in the instant application, "a subunit of the given type of subunit' is only selected "if available" as recited in claim 1 of the instant application.

Clearly, the combination of **MASON** and **AAAPA** does not show "ascertaining a given type of subunit of a configurable hardware block" and "selecting, if available, a subunit of the given type of subunit" as recited in claim 1 of the instant application. Nor does the combination of **AAAPA and MASON** teach or suggest "form pseudo-hyperblocks including a plurality of hyperblocks when implementing commands as configuration data" as recited in claim 24 of the instant application.

Moreover, a critical step in analyzing the patentability of claims pursuant to 35 U.S.C. § 103 is casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614,1617 (Fed. Cir. 1999). Close adherence to this methodology is especially important in cases where the very ease with which the invention can be understood may prompt one "to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher." Id. (quoting W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 313 (Fed. Cir. 1983)).

Most if not all inventions arise from a combination of old elements. See In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453,1457 (Fed. Cir. 1998). Thus, every element of a claimed invention may often be found in the prior art. See id. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. See id. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the appellant. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 163.5, 1637 (Fed. Cir. 1998); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125,1127 (Fed. Cir. 1984).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. See Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617. In addition, the teaching, motivation or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. See WMS Gaming, Inc. v. International Game Tech., 184 F.3d 1339, 1355, 51 USPQ2d 1385, 1397 (Fed. Cir. 1999). The test for an

implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981) (and cases cited therein). Whether the Examiner relies on an express or an implicit showing, the Examiner must provide particular findings related thereto. See Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617. Broad conclusory statements standing alone are not "evidence." Id. When an Examiner relies on general knowledge to negate patentability, that knowledge must be articulated and placed on the record. See In re Lee, 277 F-3d 1338, 1342-45, 61 USPQ2d 1430, 1433-35 (Fed. Cir. 2002).

Upon evaluation of the Examiner's comments, it is respectfully believed that the evidence adduced by the Examiner is insufficient to establish a prima facie case of obviousness with respect to the claims. Accordingly, the Examiner is requested to withdraw the rejections using the combination of **AAAPA** and **MASON**.

For example, even though **MASON** discloses a dynamically reconfigurable FPGA (which are not even mentioned in the instant application) and the **AAAPA** discloses a configurable hardware block in the form of functional hardware block 42,

there is no suggestion, teaching or motivation for making the proposed combination leaving only broad conclusory statements. Nor is there any suggestion that such a combination would be successful and capable of "ascertaining a given type of subunit" as recited in claim 1 of the instant application and required under the analysis outlined by In re Dembiczak. To the contrary, just as the crepe paper jack-o-lanterns could not be combined with the plastic orange garbage bags of In re Dembiczak, the disclosure regarding the reconfigurable FPGAs actually teaches away from the claimed limitations of the instant application.

The **GREENBAUM** reference discloses a compiling system that generates a sequence of program instructions for use in a partially reconfigurable processing unit. More specifically, **GREENBAUM** indicates that although "the main thread of control is managed by the non-reconfigurable MIPS processor" certain "loops or subroutines" cause the program to "switch temporarily to the reconfigurable FPGA to obtain an increase in the execution speed."

GREENBAUM provides no teaching or suggestion that a command block has "only one entry point and one exit point" as recited in claim 2 of the instant application. Moreover, **GREENBAUM** does not indicate that the steps of ascertaining,

selecting, and configuring subunits automatically ends "when a last command in a command block having only one entry point and one exit point has been implemented' as recited in claim 3 of the instant application.

Clearly, the combination of **GREENBAUM** with the previously discussed combination of **MASON** and **AAAPA** does not show "ascertaining a given type of subunit of a configurable hardware block" and "selecting, if available, a subunit of the given type of subunit" as recited in claim 1 of the instant application. Nor does the combination of **GREENBAUM** with the previously discussed combination of **MASON** and **AAAPA** teach or suggest "form pseudo-hyperblocks including a plurality of hyperblocks when implementing commands as configuration data" as recited in claim 24 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1 or claim 24. Claim 1 and claim 24 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on either claim 1 or claim 24.

Finally, applicants appreciatively acknowledge the Examiner's statement that claim 18 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In light of the above, applicants respectfully believe that rewriting of claim 18 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claim 1-26 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

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September 20, 2004

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